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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,765	12/03/2003	S. Brad Herner	MA-070-1	7587

7590 10/04/2005

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,765	HERNER, S. BRAD	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) *45-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 35-44* is/are rejected.

7)☒ Claim(s) *27-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I (claims 1-44) in the reply filed on 07/13/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 44-56 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07/13/05.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6, 8-26 and 35-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Feth et al. (U.S. Patent No. 4,338,622).

In re claim 1, Feth (esp. Fig. 8I) disclose a semiconductor device, comprising:

a silicide layer (230); and

a grown dielectric layer (238; column 12, line 5) on and in contact with the silicide layer, wherein the silicide layer and the grown dielectric layer are portions of the semiconductor device.

In re claim 2, Feth discloses the device of claim 1, wherein the silicide is tantalum silicide (column 11, line 54).

In re claim 3, Feth discloses the device of claim 2, wherein the grown dielectric layer comprises silicon oxide.

In re claim 6, Feth discloses the device of claim 2, further comprising a conductive layer (252; column 12, lines 38-42) on and in contact with the grown dielectric layer.

In re claim 8, Feth discloses the device of claim 6, further comprising a first silicon layer (228), the silicide layer on and in contact with the first silicon layer.

In re claims 9, Feth discloses the device of claim 6, wherein the conductive (column 12, lines 38-42) layer comprises silicon.

In re claims 10 and 11, Feth discloses the device of claim 9, wherein the conductive layer forms a portion of a Schottky diode. In re claim 11, the limitation, "after breakdown ... layer" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 12, Feth discloses the device of claim 11, wherein the Schottky diode is a portion of a memory cell (column 5, line 20 – refers to the use of the present invention as "storage cells").

In re claim 13, Feth discloses the device of claim 12, wherein the memory cell is a portion of a memory array.

In re claim 14, Feth discloses the device of claim 13, wherein the memory array is a monolithic three dimensional memory array.

Inherency dictates that any semiconductor substrate memory device, because of the repetition of transistor cells and the three dimensional structure of a semiconductor wafer, will of necessity be a three dimensional memory array.

In re claims 15, Feth discloses the device of claim 6, wherein the conductive (column 12, lines 38-42) layer comprises metal.

In re claims 16 and 17, Feth discloses the device of claim 15, wherein the conductive layer forms a portion of a Schottky diode. In re claim 17, the limitation, "wherein breakdown ... conductor" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 18, Feth discloses the device of claim 17, wherein the Schottky diode is a portion of a memory cell (column 5, line 20 – refers to the use of the present invention as "storage cells").

In re claim 19, Feth discloses the device of claim 18, wherein the memory cell is a portion of a memory array.

In re claim 20, Feth discloses the device of claim 19, wherein the memory array is a monolithic three dimensional memory array.

Inherency dictates that any semiconductor substrate memory device, because of the repetition of transistor cells and the three dimensional structure of a semiconductor wafer, will of necessity be a three dimensional memory array.

In re claims 21, Feth discloses the device of claim 6, wherein the conductive (column 12, lines 38-42) layer comprises silicide.

In re claims 22 and 23, Feth discloses the device of claim 21, wherein the conductive layer forms a portion of a Schottky diode. In re claim 23, the limitation, "wherein breakdown ... conductor" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 24, Feth discloses the device of claim 23, wherein the Schottky diode is a portion of a memory cell (column 5, line 20 – refers to the use of the present invention as "storage cells").

In re claim 25, Feth discloses the device of claim 24, wherein the memory cell is a portion of a memory array.

In re claim 26, Feth discloses the device of claim 19, wherein the memory array is a monolithic three dimensional memory array.

In re claim 35, Feth discloses the device of claim 2. The limitation, "grown by oxidizing or nitriding the silicide" is a product-by-process limitation that does not further limit the structure of this invention, thus is not given patentable weight regarding this product claim.

In re claim 36, Feth discloses the device of claim 2, wherein the conductive layer forms a portion of a Schottky diode. The limitation, "wherein breakdown ... conductor" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 37, Feth discloses the device of claim 36, wherein the Schottky diode is a portion of a memory cell (column 5, line 20 – refers to the use of the present invention as "storage cells").

In re claim 38, Feth discloses the device of claim 37, wherein the memory cell is a portion of a memory array.

In re claim 39, Feth discloses the device of claim 38, wherein the memory array is a monolithic three dimensional memory array.

In re claim 40, Feth discloses the device of claim 36, wherein the silicide is a portion of the Schottky diode.

In re claim 41, Feth discloses the device of claim 2, wherein the conductive layer forms a portion of a Schottky diode. The limitation, "wherein breakdown ... diode" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 42, Feth discloses the device of claim 41, wherein the Schottky diode is a portion of a memory cell (column 5, line 20 – refers to the use of the present invention as "storage cells").

In re claim 43, Feth discloses the device of claim 42, wherein the memory cell is a portion of a memory array.

In re claim 44, Feth discloses the device of claim 43, wherein the memory array is a monolithic three dimensional memory array.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feth as applied to claim 2 above, and further in view of Harari (U.S. Patent No. 4,417,325).

In re claims 4 and 5, Feth discloses the device of claim 2, but does not expressly disclose the dielectric layer comprising silicon nitride. Harari discloses a silicon nitride layer alternatively being used in place of silicon oxide. It would have been obvious for one skilled in the art at the time of the invention to use a silicon nitride layer as disclosed by Harari in place of the silicon oxide layer of Feth for the purpose, for example, of maintaining good isolation between conductive layers (Harari; column 4, lines 32-37).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Feth et al. (as above).

In re claim 7, Feth discloses the device of claim 6, wherein the grown dielectric layer is of "varying thickness" (column 12, line 10) and characterized as "thin" (column 12, line 25), but a specific empirical value is not given. Based on such a disclosure, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the layer about or less than 50 angstroms thick, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Allowable Subject Matter

8. Claims 27-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The semiconductor device comprising at least a titanium nitride layer as the conductive layer on and in contact with the grown dielectric layer is neither anticipated nor obvious over the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815